DARPA's ERI – Strengthening US Defense Electronics Advantage

By John Haystead

Although Congress chose to completely bypass the issue in the recently-signed FY2022 National Defense Authorization Act (NDAA), the Defense Advanced Research Projects Agency's (DARPA's) Electronics Resurgence Initiative (ERI) still shows the way forward to addressing the greatest vulnerability to the Nation's strength and security – loss of semiconductor technology dominance. The ERI had its genesis nearly five years ago with the recognition that continued US leadership in microelectronics was threatened in both the defense and commercial sectors.

The DARPA Microsystems Technology Office (MTO) held its fourth annual ERI Summit at the end of October last year. MTO's core mission is the "development of high-performance, intelligent microsystems and next-generation components to enable dominance in National security C4ISR, EW, and DE applications." Although the 2021 ERI Summit itself was held virtually, the importance of the subject matter discussed was very much real-world. This year's summit revolved around the launching of ERI 2.0, the latest iteration of the ERI umbrella program.

Hosting the Summit's opening technical session, Dr. Carl McCants, ERI Special Assistant to DARPA Director, provided an historical perspective of the event. The ERI officially began in 2018 with its first summit in San Francisco, California, where a number of factors were identified as driving the

initiative. These included the offshore migration of advanced semiconductor manufacturing capability, the exploding complexity of microsystems across the board in state-of-the-art processors and system-on-chip system and package configurations, and the emergence and recognition of hardware security threats in both consumer and defense applications.

From these factors, six focus areas were identified: Increasing Information-processing density and efficiency, accelerating innovation in AI hardware to make decisions at the edge faster, overcoming the inherent throughput limits of 2D microelectronics, mitigating the skyrocketing costs of electronic design, overcoming security threats across the entire hardware lifecycle and revolutionizing communications 5G and beyond.

Said McCants, “Today these factors are even stronger drivers than they were when ERI was first initiated, with new trends emerging and a consensus in the need for action to address these trends.” Among these, he pointed to the enormous offshore investments in commercial electronics by near-peer allies and adversaries “which have only grown since the start of ERI, particularly as manifested by the consolidation of leading-edge silicon manufacturing and an increasing footprint into state-of-the-art packaging by pure-play foundries.” McCants also noted that the integrity of the microelectronics supply chain has also been of growing concern spurred by the disruptions of COVID-19 and the global nature of the supply network, as well as the formation of multinational alliances for 3D heterogeneous integration (3DHI) R&D and manufacturing.

ERI 2.0 LAUNCHES

A number of assumptions informed the planning for ERI 2.0. These were the recognition that maintaining US supremacy in semiconductor technologies over the long-term will demand a national investment in disruptive technologies; the fact that

the scaling of transistors is unlikely to persist much further (and in any case will not drive future microelectronic innovation), meaning future microelectronics will instead be tied to the ability to design, fabricate, test and model the performance of complex 3D assemblies composed of heterogeneous microelectronic technologies; and that lab-to-fab capability represents an opportunity to accelerate and re-shore future manufacturing. Says McCants, "The result is that ERI must continue to strategically invest and seed new approaches to technology to maintain the US position in electronics systems and technology R&D."

Well before the creation of the ERI, the threat to the US lead in semiconductor technology was well recognized, or at least, it should have been. As referenced by McCants, the President's Council of Advisors on Science and Technology (PCAST) issued a Jan. 2017 report stating that "U.S. semiconductor innovation, competitiveness and integrity face major challenges. Semiconductor innovation is already slowing as industry faces fundamental technological limits and rapidly evolving markets. Now a concerted push by China to reshape the market in its favor, using industrial policies backed by over $100 billion in government-directed funds, threatens the competitiveness of U.S. industry and the national and global benefits it brings."

Reinforcing the point, Dr. Jason Boehm, Director, Program Coordination Office, National Institute of Standards and Technology (NIST), a physical sciences laboratory and non-regulatory agency of the United States Department of Commerce, observed during his presentation, that "over the past several decades, what we've seen is that our capacity for manufacturing advanced microelectronics and semiconductors has been on the decline. At one point we were about 37% of the global manufacturing capacity and now we're at about 12%. While global manufacturing capacity is projected to increase quite significantly because of huge demand, we find that we're in a very difficult competitive position and unless we take

actions to incentivize construction of fabrication facilities here in US, it's projected that we will continue to drop in share of global manufacturing capacity."

The PCAST report laid out a plan for strengthening US leadership in semiconductors: "Promoting US interests will ultimately require a strong focus on advancing semiconductor innovation. This demands a three-part strategy that pushes back against innovation-inhibiting Chinese industrial policy, improves the business environment for US-based semiconductor producers, and helps catalyze transformative semiconductor innovation over the next decade."

IF WE (CAN'T) BUILD IT, THEN WHAT?

The recognition of the importance of maintaining dominance in microelectronics technologies has been increasing dramatically within the DOD and other Government agencies with substantial investment in microelectronics identified as a key priority. Nevertheless, so far this recognition, and the actual spending of real money on the problem, have been pretty much two different things entirely.

To begin with, as pointed out by Boehm, "To make sure that we have a firm footing in domestic manufacturing and a robust R&D ecosystem, leaders in industry and Congress got together and worked on the programs called out in the CHIPS for America Act (CHIPS Act) as part of the FY2021 National Defense Authorization Act (NDAA)."

Said Boehm, "One key goal of the CHIPS Act was to make sure that we have, and are able to protect and extend, our US semiconductor technology leadership, and that we continue to have the investment in early stage R&D and the infrastructure to help translate and move that to development, prototyping and capturing the manufacturing course location. We want to ensure that we have a secure supply of chips for critical commercial economic sectors, as well as unique defense needs.

This means ensuring that the US captures its share of projected growth in fabrication facilities across the globe so that we have a significant and stable chip manufacturing sector at the leading edge domestically to meet our critical needs, as well as to contribute to the global market. Right now, the great majority of this capability is located in Taiwan and South Korea, and over the past year, we've seen the challenges posed by the combined impacts of the pandemic, issues surrounding National disasters, and other factors creating microelectronics shortages and revealing the fragility of the global supply chain."

"Ultimately," says Boehm, "the goal is to promote a long-term, economically-viable domestic US semiconductor industry with a robust R&D infrastructure, manufacturing sector, and supply chain. At the end of the day, if we lose that manufacturing footprint and it all moves offshore, then we will lose key capabilities and work force that will further erode our leadership in research and innovation. The Chips Act programs collectively provide us all the tools we need to be able to address this challenge."

The 2021 NDAA authorized funding for the CHIPS Act, which included a number of sections. Section 9902 of the act authorized funding for the Commerce Department Financial Assistance Program, including grants for domestic semiconductor manufacturing and R&D. Section 9906 authorized the establishment of a National Semiconductor Technology Center (NSTC) (9906c) and section 9906d authorized funding for the National Advanced Packaging Manufacturing Program.

Says Boehm, "With regard to the National Advanced Packaging Manufacturing Program, this is really seen as a force multiplier. We realize that heterogeneous integration and advanced packaging will be a huge driver for innovation, and this is an area that the US absolutely must capture a leadership position."

Boehm also sees the NSTC as one of the core foundational pieces of the CHIPS Act. Envisioned to be an entity that can help, accelerate and drive research in advanced semiconductor manufacturing processes, design and packaging, the Center is expected to address Technology Readiness Levels (TRLs) 3-8, supporting access to design tools, robust prototyping and fabrication tools, advanced packaging, assembly and test capabilities and facilities, as well as providing for workforce development. Boehm says, they're "still in the process of talking with all the stakeholders and gathering input," but he expects it would be established through a competitive process. "As a piece of the National infrastructure, the NSTC must have a balance between operational independence and industry involvement."

Another area addressed in the CHIPS Act is the enhancement of metrology R&D. "This is critical for any manufacturing industry," says Boehm, "and we're looking at ways to expand our capabilities both in terms of the types of facilities that we can offer to the community and how we can align these efforts to work best with the NSTC, Manufacturing USA Institute and other programs to address both front- and back-end metrology challenges, as well as in assembly and packaging, test issues, and security and authentication along with automation and virtualization processes."

As an example of some of the things that NIST already does in the field of metrology, Boehm points to the unique facilities that they have available, including the Synchrotron Ultraviolet Radiation Facility (SURF). One of only two such facilities in the world, Boehm says it has "played a critical role in the development of advanced UV lithography technology since the 1990s." NIST is also always looking to contribute new reference materials and material test structures to enhance metrology capabilities.

As Boehm noted, all of these initiatives are designed to be interconnected and to "address a common set of challenges

across the semiconductor/microelectronics technology ecosystem. We can't treat them as stovepipes working in isolation." Although today, Boehm points to existing innovative research programs in microelectronics from DARPA, NSF, DOE, as well as in university and national labs, "it's often difficult to transition those new innovations into manufacturing. We're lacking some of the necessary infrastructure, resulting in many of these would-be-successful achievements instead ending in the dreaded 'valley of death.' The CHIPS act is intended to fill this void and help avoid that result."

One example of how this interconnection could be achieved, says Boehm, is by tying together a broader set of R&D programs at the NTSC that will be focused on prototyping and scaling such capabilities. "And, since we'll need to be able to access fabrication facilities, recipients of these funds will be encouraged to allocate a certain number of wafer runs for NSTC-oriented projects."

SHOW ME THE MONEY!

The current status of the CHIPS Act provides a very clear illustration of the fact that authorization is not the same as the actual appropriation of funds.

In June 2021, the Senate passed an omnibus $250 billion US Innovation and Competition Act (USICA – S.1260) intended to be a part of the FY2022 NDAA. Included in this bill was a $52 billion appropriation to fund the CHIPS Act initiatives including $39 billion over five years for section 9902 ($19 billion in FY2022 and $5 billion per year for the following four years). It also included $2 billion in FY2022 for section 9906 for the NSTC plus $500,000 for other related R&D, and $5.5 billion shared with the Advanced Packaging and other programs ($2 billion in FY23, $1.3 billion in FY2024, and $1.1 billion in FY2025 and FY2026).

The omnibus nature of the appropriation, beyond just CHIPS programs, however, turned out to be a major problem. Although the CHIPS Act had passed easily with bi-partisan support and a common plan between the House and Senate, the much broader USICA legislation was a different story, with partisan political issues and the House having its own version of how, and how much, of this funding would be provided. As a result, in order to move forward with approval of the overall NDAA, the Senate withdrew the USICA portion. And, that is where things currently stand.

If, however, the CHIPS Act funding is indeed eventually provided, NIST expects to fund a number of additional activities in the space, such as development of a plan for increasing commercialization of IP developed by the DOD, the development of multiple models of public/private partnerships, and a national network for microelectronics R&D to enable the smooth laboratory-to-fabrication transition of microelectronics innovations. Says Boehm, “Each participating institute will follow a common model providing a common set of shared-use facilities, conduct applied research and also provide capabilities for workforce training.”

Another program authorized under the CHIPS Act, that the Commerce Department would be responsible for, is the creation of a Manufacturing USA Institute or multiple institutions specifically focused on the unique manufacturing challenges of the semiconductor industry. The overall program has been around for many years, establishing core research hubs and industry-led consortia and public/private partnerships that are focused on different manufacturing industry sector R&D challenges. Right now, there is a network of 16 institutes across the country which NIST coordinates supported by a combination of NIST and DOE/DOD funding. Says Boehm, “It’s definitely fitting to have one or more addressing the unique challenges of semiconductor manufacturing.”

Even without having received CHIPS Act funding yet, NIST is

nevertheless planning a CHIPS Act Program Office within NIST to provide the infrastructure to support these programs. “When these are funded,” says Boehm, “there will be a lot of opportunity for jobs and where we will need the community’s help, such as leadership for programs etc.”

Congress is also in the early consideration phase of legislation called the Facilitating American-Built Semiconductors Act (FABS Act), which would establish a semiconductor investment tax credit. First introduced in June of 2021, it is endorsed by the Semiconductor Industry Association stating that “the FABS Act should be expanded to include expenditures for both manufacturing and design to help strengthen the entire semiconductor ecosystem.”

DARPA ERI KEEPS US IN THE GAME

While the desperately needed, funding authorized but not yet appropriated in the CHIPS Act and the proposed FABS Act remain in limbo or planning stages. DARPA MTO and the ERI are nevertheless making important progress in keeping the US at least in a potentially competitive position in advanced microelectronics technology.

As pointed out by Dr. McCants at DARPA, one of the main purposes of holding an annual ERI summit is to present current work and note accomplishments. “The intent is to provide benchmarks for the progress we’re collectively making and to encourage feedback on the technical emphasis and where we might be going in future.” As part of this, McCants notes that ERI has increased participation of non-traditional partners from commercial industry in DARPA programs, fostering collaborative projects involving six of the top 10 semiconductor sales leaders, all five leading defense contractors and all of the top ten research universities (per *U.S. News & World Report* ranking). “We continue to strive to increase the base of those entities participating in our

funded research."

Among the many specific successes over the past year, McCants points to the Hierarchical Identify Verify Exploit (HIVE) program, whose processor architectures deliver more than 100 times faster speeds than standard CPUs and GPUs; the development of programmable hardware architectures to increase processing efficiency under the Software Defined Hardware (SDH) program; the integration of machine learning into tools for end-to-end electronic design under the Intelligent Design of Electronic Assets (IDEA) program; data privacy research to process information while it remains encrypted such that the data is protected under the Data Protection in Virtual Environments (DPRIVE) program; hardware security architectures to protect systems against whole classes of hardware vulnerabilities exploited through software, not just individual vulnerability instances, through the System Security Integration Through Hardware and Firmware (SSITH) program; integration of an FPGA core with a photonic transceiver in a multichip module in the Photonics in the Package for Extreme Scalability (PIPES) program; and early demonstrations of 22nm finFETs for specific defense industrial base applications. ERI has also provided open licensing with commercial technology vendors for DARPA research through the "DARPA Toolbox" Initiative.

In addition, McCants notes that over the past year DARPA has also created several new ERI programs in computing, algorithms, filters and heterogeneous integration. Among these is the Low Temperature Logic Technology (LTLT) program, which will develop low temperature (~77°K) device technology to achieve a factor of 25 improvement in performance and power compared to state-of-the-art room temperature CPUs; the Quantum-Inspired Classical Computing (QuICC) program to develop quantum- inspired solvers for a factor of 500 improvement over existing techniques in computational efficiency for a broad range of "hard optimization problems;"

the Compact Front-end Filters at the Element level (COFFEE) program that will create an integral RF filter technology to mitigate the interference vulnerabilities of wideband Active Electronically Scanned Arrays (AESAs) operating in congested RF environments; and the Electronics for G-band Arrays (ELGAR) program to develop the integration technologies needed to create compact, high-performance G-band-array front ends to enable DOD communication and sensing phased array systems.

WHAT WILL ERI 2.0 BRING?

Looking at the future and specifically the future for ERI 2.0, McCants says, “We first have to look at what we’ve already learned. Among these is that it is possible to engage the academic, commercial, and US Government microelectronics communities in relevant, cutting-edge, dual-use research projects. We’ve also learned that it is possible to provide leap-ahead capabilities in computational efficiency, heterogeneous integration, hardware security, electronics design, AI components and secure communications through these collaborations that benefit both the US Government and private sector. However, we’ve also learned (or relearned) that maintaining technical advantage will require continuous innovation.”

McCants says the next question is, “What are the trends today both in applications and technology and the industrial base that should shape our thinking about future R&D?” Pointing to application trends they’ve considered over the past year, such as passive sensing and adaptive electronic warfare (EW), McCants observes that other technology trends include novel computing and manufacturing and prototyping. Among industrial-base trends, he points to re-shoring manufacturing, heterogeneous integration proliferating in products, and computing-at-the-edge AI growth rates in various commercial market sectors. “Again, the question is, what opportunities should we prioritize in planning for the future?”

To answer this question, McCants observes that DARPA's mission is to "prevent technological surprise as well as to create technological surprise when an opportunity is identified." This, says McCants, typically involves a longer time horizon than when focusing on translating commercial advances for DOD needs. So, for ERI going forward, this means asking questions like: What, as gains from transistor scaling continue well into the next decade, new manufacturing paradigms will appear? What fabrication techniques will be associated with disruption in performance? As we reach the classical quantum limit in transistor dimensions, and as the importance of microscale packaging increases, another question is, what packaging and assembly infrastructure and tool capabilities will be needed? What would support automating more of the manufacturing processes beyond the front-end foundry? How might an increase in the testing and validation activities for complex Systems on Chips (SOCs) provide feedback to the research more quickly, and what aspects of testing might be customized and automated through machine learning, taking advantage of predictive analysis?

McCants says all of these thoughts – combined with well-timed studies, analyses and a myriad of conversations – led to the assumptions described earlier in the planning of ERI 2.0. "Taking all of this into account, with ERI 2.0, we will continue innovating the next generation of microelectronics through the initial six areas of the initiative. But we will also be adding two new areas – R&D for Advanced Manufacturing and Electronics for Harsh or Extreme Environments."

R&D for Advanced Manufacturing will include the design, assembly, testing and digital emulation of 3DHI microsystems with an emphasis on the following: multichip/multi-technology assembly and packaging, tools for design, simulation and test, security, 3DHI interconnects, thermal management and power delivery. It will also pursue next-generation microelectronics prototyping. Says McCants, "We expect this will do the

following: reduce cycle time for R&D and pilot manufacturing for 3D electronics assembly, ensure secure domestic supply chain with a domestic facility and provide the capabilities driven by future industry needs. Next, it will provide technology for advanced packaging and assembly with the potential for significant cost reduction in microsystems, and it will emphasize design innovations and enhance the use of manufacturing automation in the package, assembly and testing process."

The second new focus area for ERI 2.0 – Electronics for Harsh or Extreme Environments – will recognize and examine how high radiation, extreme temperature, high power (whether voltage or current) each present their own unique challenges and opportunities. Individual presentations at the 2021 ERI Summit specifically addressed both of these new ERI 2.0 focus areas.

The ERI program forms a critical piece of US strategy for semiconductor technology. McCants recognizes this when he says "As we prepare for the future, we definitely expect to have many new opportunities for coordination and collaboration with other Federal partners, academia, and industry."